



## WEST Search History

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DATE: Monday, September 27, 2004

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<input type="checkbox"/>	L14	L13 not l6	5
<input type="checkbox"/>	L13	L12 and (processor or microprocessor or CPU or multiprocessor)	11
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<input type="checkbox"/>	L10	(5847998  5867430  6016270  6088264  6097666  6111787)! [pn]	6
<input type="checkbox"/>	L9	(5847998  5867430  6016270  6088264  6097666  6111787)! [pn]	6
<input type="checkbox"/>	L8	(3471838  5229972  5245572  5307314  5361343  5367494  5420997  5436863  5475634  5502683  5513139  5553016)! [pn]	12
<input type="checkbox"/>	L7	(5245572  5361227  5361343  5426603  5483486  5572466  5590074  5625595  5648929  5732030  5748528  5751634  5796657  5867430  5917744  5936884  5949713)! [pn]	17
<input type="checkbox"/>	L6	L5 and "processors"	6
<input type="checkbox"/>	L5	l1 or l3	9
<input type="checkbox"/>	L4	l1 and l3	0
<input type="checkbox"/>	L3	l2 or 5847998.pn.	4
<input type="checkbox"/>	L2	(5657292 or 5867430 or 6081878).pn.	3
<input type="checkbox"/>	L1	(6088264 or 6081450 or 6418506 or 5732017 or 6240040).pn.	5

END OF SEARCH HISTORY

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Generate Collection

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L14: Entry 5 of 5

File: USPT

Apr 26, 1994

DOCUMENT-IDENTIFIER: US 5307314 A

TITLE: Split read/write dynamic random access memory

Brief Summary Text (15):

Instructions, comprising an output enable (OE) signal and a write enable (WE) signal, generated in a central processing unit (CPU) control the read and write operations of a typical DRAM. (Throughout this discussion designations OE and WE will be considered the OE and WE signals unless stated otherwise, another option being the physical OE and WE outputs.) The active and inactive logic states of the OE and WE instructions determine whether data is written to or read from a memory cell. In order to read data from a memory cell, OE needs to be in an active logic state and WE needs to be in an inactive logic state. In order to write data into a memory cell, WE needs to be in an active logic state and OE needs to be in an inactive logic state. Both the read and write operations are preceded by an active row address strobe (RAS) signal and also require an active column address strobe (CAS) signal. In typical DRAMs, the WE and the OE are not activated at the same time. This is because the data ports are shared for input and output data. The DRAM logic inhibits the condition of both the OE and WE signals active at the same time by either not allowing it or by disabling the DRAM's ability to transmit data to the output.

Brief Summary Text (30):

This device can also be used in a dual processor system having a shared memory for communicating between the processors. It can also be used for special graphics functions such as digital television and frame buffers for television and communication systems.

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